

# Self-Aligning Planarization and Passivation for Integration Applications in III–V Semiconductor Devices

Hilmi Volkan Demir, Jun-Fei Zheng, Vijit A. Sabnis, Onur Fidaner, *Student Member, IEEE*, Jesper Hanberg, James S. Harris, Jr., *Fellow, IEEE*, and David A. B. Miller, *Fellow, IEEE*

**Abstract**—This paper reports an easy planarization and passivation approach for the integration of III–V semiconductor devices. Vertically etched III–V semiconductor devices typically require sidewall passivation to suppress leakage currents and planarization of the passivation material for metal interconnection and device integration. It is, however, challenging to planarize all devices at once. This technique offers wafer-scale passivation and planarization that is automatically leveled to the device top in the 1–3- $\mu\text{m}$  vicinity surrounding each device. In this method, a dielectric hard mask is used to define the device area. An undercut structure is intentionally created below the hard mask, which is retained during the subsequent polymer spinning and anisotropic polymer etch back. The spin-on polymer that fills in the undercut seals the sidewalls for all the devices across the wafer. After the polymer etch back, the dielectric mask is removed leaving the polymer surrounding each device level with its device top to atomic scale flatness. This integration method is robust and is insensitive to spin-on polymer thickness, polymer etch nonuniformity, and device height difference. It prevents the polymer under the hard mask from etch-induced damage and creates a polymer-free device surface for metallization upon removal of the dielectric mask. We applied this integration technique in fabricating an InP-based photonic switch that consists of a mesa photodiode and a quantum-well waveguide modulator using benzocyclobutene (BCB) polymer. We demonstrated functional integrated photonic switches with high process yield of >90%, high breakdown voltage of >25 V, and low ohmic contact resistance of  $\sim 10 \Omega$ . To the best of our knowledge, such an integration of a surface-normal photodiode and a lumped electroabsorption modulator with the use of BCB is the first to be implemented on a single substrate.

**Index Terms**—Integrated optoelectronics, passivation, semiconductor device manufacturing, wafer-scale integration.

## I. INTRODUCTION

**I**n today's III–V semiconductor technology, 50%–80% of the total cost typically comes from device packaging. Such high packaging cost means we should minimize chip packaging in

Manuscript received January 1, 2003; revised November 2, 2004. This work was supported in part by Intel Corporation and by PTAP (funded by the National Science Foundation and the Defense Advanced Research Projects Agency).

H. V. Demir is with the Edward L. Ginzton Laboratory and Solid State and Photonics Laboratory, Stanford University, Stanford, CA 94305 USA and also with Nanotechnology Research Center, Bilkent University, Bilkent Ankara TR-06800 Turkey (e-mail: volkan@bilkent.edu.tr; volkan@stanfordalumni.org).

J. F. Zheng is with Intel Strategic Technology, Intel Corporation, Santa Clara, CA 95052 USA.

V. A. Sabnis is with Translucent, Inc., Palo Alto, CA 94303 USA.

O. Fidaner, J. S. Harris, Jr., and D. A. B. Miller are with the Edward L. Ginzton Laboratory and Solid State and Photonics Laboratory, Stanford University, Stanford, CA 94305 USA.

J. Hanberg is with GIGA ApS, Intel Corporation, DK-2740 Skovlunde, Denmark. Digital Object Identifier 10.1109/TSM.2004.841834

any subsystem incorporating III–V semiconductor devices. This might be achieved, for example, by integrating multiple III–V devices on a single chip. This is, however, not a straightforward task. One of the difficulties stems from a III–V device passivation requirement that creates planarization and interconnection problems. In conventional etch-back planarization methods [1], it is challenging to achieve planarization across the entire wafer so that the integrated device sidewalls are all sealed and passivated, especially where the top layers are only submicrometer thick. In this paper, we introduce a novel wafer-scale integration method using a polymer that passivates the sidewalls all the way to the top of the layered heterostructure across the wafer. This method provides self-aligning planarization and passivation across the wafer.

In our integration method, the sidewalls of III–V devices are completely passivated with a polymer that self-planarizes flush with the device top to an atomic flatness in the vicinity of the devices across the entire wafer. The process is illustrated in Fig. 1 and consists of the following steps: 1) defining a dielectric hard mask on the (epitaxial) wafer, which is retained for the subsequent steps; 2) defining the semiconductor device area with the use of the hard mask by vertically etching the unmasked parts of the wafer; 3) selectively etching the sidewalls of the semiconductor structure in the lateral direction to create an undercut beneath the hard mask; 4) sealing and passivating the sidewalls of all device layers under the hard mask with a spin-on polymer; 5) etching back the cured polymer past the top level of the hard mask with an anisotropic dry etch; and finally 6) removing the hard mask to create a passivation structure, with the polymer around the device perimeter completely level with the device top. Depending on where the polymer etch-back process is stopped with respect to the hard mask and the semiconductor device, various final polymer profiles might be obtained for different purposes.

The undercut renders this integration technique robust and insensitive to spin-on polymer thickness, polymer etch nonuniformity, and device height difference. The undercut structure also protects the polymer under the hard mask from etch-induced damage. Furthermore, when the hard mask is removed, a clean, polymer-free device surface is left for metallization. Also, if desired, stopping the polymer etch back within the hard mask thickness, self-aligned via-like structures can be obtained for easy metallization [2]. In a similar approach, even without the use of an undercut, a relatively thick hard mask allows a more relaxed margin for the etch depth of the polymer and a larger thick-

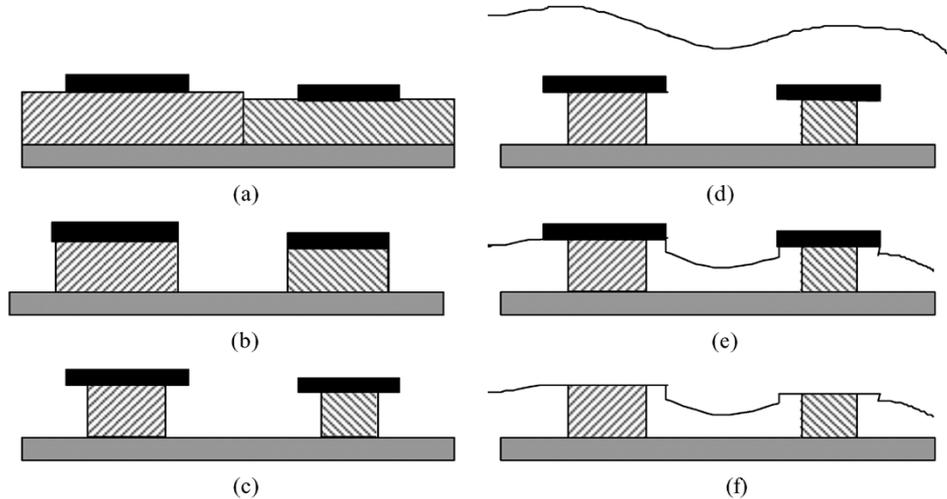


Fig. 1. Illustration of the self-planarizing passivation process sequence: (a) Start with defining hard masks on the (epitaxial) wafer, which may consist of different selectively grown regions, (b) define device areas by vertical etching, (c) selectively remove the device material underlying the perimeters of the hard masks to create undercuts, (d) while retaining the hard masks, seal the device areas using a spin-on polymer, (e) etch back the cured polymer past the top levels of the hard masks, and (f) remove the hard masks.

ness variation tolerance. This hard-mask-assisted planarization further makes it possible to metallize small devices surrounded with the passivation polymer and route and isolate electrical interconnects between these metallized devices over the polymer.

We made use of this new integration method to fabricate an InP-based optically controlled optoelectronic switch incorporating a dual-diode structure, a mesa photodiode and a waveguide quantum-well modulator tightly integrated on the same substrate [3]–[5]. We used benzocyclobutene (BCB) as the passivation polymer [6]. We used either silicon nitride or silicon oxide as the hard mask. We demonstrated functional integrated photonic switches with high process yield of  $>90\%$ , high breakdown voltages of  $>25$  V, and low ohmic contact resistances of  $\sim 10 \Omega$ .

## II. DIFFICULTIES WITH CONVENTIONAL PASSIVATION AND PLANARIZATION TECHNOLOGY

Current III–V semiconductor device fabrication typically requires the epitaxial growth of III–V compound device materials with various alloy contents on a III–V substrate [7]–[9]. Such epitaxially grown III–V heterostructures can be on the order of nanometers to micrometers in thickness. When selectively removing material through vertical etching to define semiconductor devices [10], the device sidewalls are left exposed, creating chemically active dangling bonds and introducing surface states. This gives rise to leakage and long-term stability problems. Therefore, proper passivation of device sidewalls is required [11] and, in some cases, subsequent planarization of the passivation layers is also necessary [1].

The current planarization techniques of polymer-based passivation layers typically rely on one of two main methods. The first method requires spinning the polymer on the predefined semiconductor devices and etching it back to be level with the device top [1]. The second method employs another mask step to allow for selectively etching the polymer, only for small areas defined by photoresist or dielectric mask openings on top of

the semiconductor devices, to form via structures through the polymer [12].

There are several potential difficulties and problems during fabrication with the first method.

- 1) The polymer etch depth has to be precise around the device top level, requiring an exceedingly careful design of etch recipes and painstaking characterization of etch rates. In some cases, even *in situ* etch depth monitoring, such as thin-film thickness measurement using a laser, is required. However, the laser etch-depth monitor only returns local information, which is not necessarily consistent with the etch depth at all other locations on the wafer. This problem is further intensified due to the requirement of tight etch-depth precision often set by the epitaxial layer thicknesses, which might be of submicron thickness. Also, the polymer depth variations formed during spin-on and subsequent polymer reflow during curing exacerbates the difficulty of obtaining a precise etch depth all through the wafer. This leaves the process extremely dependent on the degree of planarity of the polymer and its cured film thickness profile across the wafer. Furthermore, the polymer etch rate is nonuniform across the wafer, for instance, faster closer to wafer edges. Likewise, the semiconductor devices that are to be passivated and planarized are also typically not uniform across the wafer to start with, again because of their nonuniform semiconductor etching. Processing small pieces as required with III–V materials in some cases only amplifies these problems.
- 2) After the polymer etch back, a residual layer of polymer may remain on the top surface of the semiconductor device in some processes. In this case, this thin-film polymer layer is typically extremely difficult to remove because of carbonization during the etching process or due to possible particle contamination that masks the polymer film. Overetching to remove this thin film can unintentionally expose the sidewalls as well. Such a residual polymer unfavorably increases contact resistance.

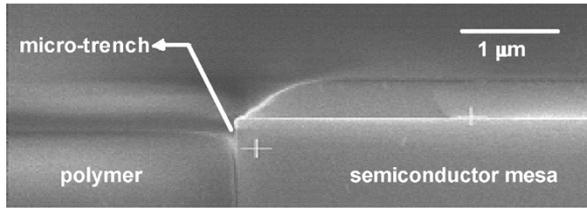


Fig. 2. Cross-sectional SEM picture to illustrate the formation of microtrenches along the interface of the polymer and a semiconductor device during the polymer etch-back process.

- 3) Toward the conclusion of the etch-back step, faster etching may occur at the polymer/semiconductor-side-wall interface due to an enhancement in the local electric field. This leads to the formation of unwanted trenches in the polymer along the sidewalls. Depending on the severity of the microtrenching, sidewalls might be exposed significantly, causing the passivation to fail, or metal might fill the trench during metallization with possible short circuits as a consequence. Fig. 2 shows a scanning electron micrograph of such microtrenches formed in the polymer along an InP waveguide ridge during the etch-back process.
- 4) During spin-on, the polymer might develop imperfections such as bubbles or voids in some processes. These imperfections might grow to form microdefects during etch back, providing additional causes for accidental electrical shorting. Fig. 3 shows a typical atomic force microscope scan across the cured polymer after its etch back to demonstrate the formation of microvoids in the polymer around a semiconductor device during the etch back.
- 5) On-chip III-V device integration might end up with the production of devices with different heights over the substrate level, for example, due to selective-area epitaxial growths. This makes the creation of a passivation layer perfectly planar with all individual devices an arduous task.

As a result, these aforementioned difficulties and possible problems prevent the fabrication process from being robust across the wafer, and thus significantly reduce the device yield.

The second method of via formation (masking for selective polymer etching) is impractical if the device itself has lateral dimensions that are too small. Among the examples of such small-size devices are III-V waveguide ridges that are a few micrometers wide, low-capacitance high-speed photodiodes that are a couple of micrometers across, and grating structures that are submicrometers wide. In these cases, since the via has to be even smaller, this method adds an expensive extra mask step to the process, a step that also requires proper alignment of the via to the device. In research environments, submicron lithography is not always available, and creating a via above these small structures is difficult. Such strict via alignment might require the use of expensive step aligners that may need to provide alignment precision of  $<0.1 \mu\text{m}$ .

In order to obtain a reliable and robust process, a new planarization and passivation technique that allows complicated

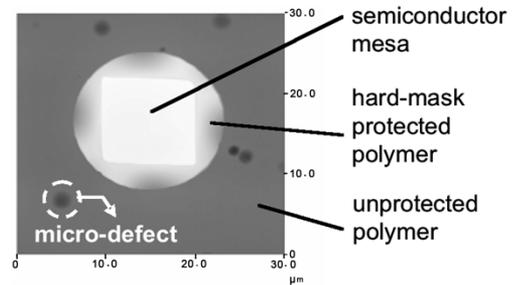


Fig. 3. AFM scan showing the formation of microvoids in the polymer around a semiconductor device during the polymer etch back.

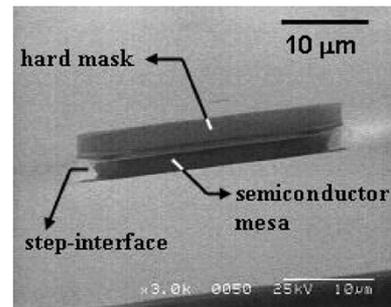


Fig. 4. A SEM picture of a semiconductor device mesa with its hard mask retained on the top.

structures to be produced and integrated on a single wafer in a single step is required.

### III. OUR NEW METHOD: SELF-ALIGNING HARD MASK ASSISTED PLANARIZATION AND PASSIVATION

To define devices on an epitaxial structure, it is a well-established technique to form areas of hard masks (typically of silicon nitride or silicon oxide) on the unprocessed (epitaxial) III-V wafer. After subsequent etching to create device mesas, such a hard mask is usually removed at some point, prior to polymer spinning, to continue with the processing of planarization and metallization.

In our method, we retain the hard mask on top of the formed devices, as shown in Fig. 4. Additionally, we intentionally undercut the hard mask by laterally etching the device sidewalls. The importance of the undercut formation is that it causes the hard mask to overhang, creating a roof over the device. An undercut with a micrometer-range lateral depth into the device area is sufficient. There is no thickness requirement on the hard mask beyond that it should stand up to the polymer spinning and the polymer etch-back processes. In our application, we used  $0.1\text{--}0.85\text{-}\mu\text{m}$ -thick hard mask layers, and  $1\text{--}3\text{-}\mu\text{m}$  deep undercuts.

Once this hard mask roof has been formed, processing continues conventionally, with the polymer spin-on and curing. During the spin-on, the polymer covers the wafer and fills under the overhang of the hard mask roof as well. Any polymer that would fill under the overhang, such as photoresist, can be used. There is no self-planarity requirement for the polymer; it is not necessary to use a specially formulated polymer with an engineered viscosity that results in planar films after curing.

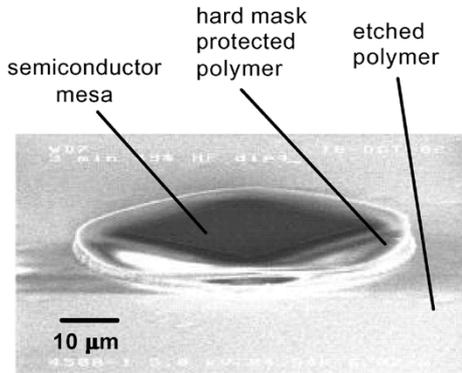


Fig. 5. SEM picture of a semiconductor device quasi-planarized with a passivation polymer etched back past the hard mask.

The polymer etch back is then initiated, to be stopped at a chosen point. Depending on what the fabrication is intended to achieve, different choices can be made for the stopping point as soon as the hard mask is exposed.

By stopping the etch back past the hard mask, and selectively wet or dry etching the hard mask, a protected locally planar layer of polymer surrounding the device and passivating the sidewalls is obtained, as shown in Fig. 5. The desirable property of the resultant structure is that the passivation layer is now perfectly flat around the perimeter of the device, since the polymer fills in the undercut and is protected under the hard mask roof during the etch back. Thus, self-planarization around the device is achieved without relying on the etch-back process or the initial planarity of the polymer after spin-on or without requiring excessive precision during etch back. There is no residual polymer left on the device, where the hard mask has been covering. This method also protects against microtrench formation and other kinds of microdefects, since the hard mask protects the polymer right against the sidewalls of the device in the undercut, as pictured in Fig. 6, during etch. Microdefects are not observed in the surrounding polymer area that is protected by the hard mask during the etch back, but only in the far polymer region that is unprotected, as observed in Fig. 3.

In this technique, the limitation on the stopping point of the polymer etch back comes from a possible subsequent top metallization, i.e., the down-step of the polymer surrounding the area that is protected by the roof has to be shallow enough to be completely covered by the metal in case the metal needs to be routed over the polymer. Such micrometer-sized down steps can be easily covered using thick metal evaporation, metal plating, and tilted metal deposition in case of directional (e.g., e-beam) deposition. To circumvent this limitation, it is also possible to stop the polymer etch back within the thickness of the hard mask, as shown in Fig. 6. In this case, once the mask has been stripped, a self-aligned via-like opening is obtained for easy metallization. While the conventional via method outlined in the previous section also protects against trenching and microdefects, the advantages of our method are that it is self-aligning and does not require an extra mask step [2].

If there are devices of different heights fabricated on the wafer, hard masks are kept on all of them until after the polymer etch back. The etching is allowed to continue at least until the level of the lowest device's hard mask is reached, while the

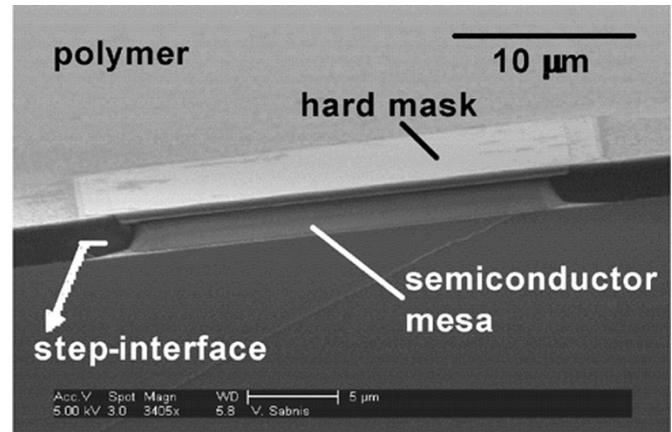


Fig. 6. SEM picture of a semiconductor device quasi-planarized using a passivation polymer with its etch back stopped within the thickness of the hard mask.

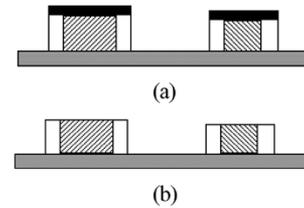


Fig. 7. Illustration of vertical thin-film sidewall passivation of semiconductor devices using a spin-on polymer (with no planarity property): (a) after etching back the polymer completely and (b) after removing the hard masks.

masks over higher devices keep protecting the polymer around them. Thus, once the hard masks are removed, perfect local planarization is still achieved for each device. Hence, this method provides multilevel quasi-planarization reliably across a wafer in a single etching step. We used this technique to planarize devices made of different epitaxial layers with a height difference of  $0.5 \mu\text{m}$  locally in their vicinity all at once in a single step.

As a matter of fact, even when there are no devices of different heights manufactured intentionally on the wafer, due to depth variations during the polymer spin-on step and varying etch rates along the wafer, it is inevitable that the polymer etch back will actually stop at different levels for different wafer regions. But, as described in the different-device-height case above, this is not a problem; the process will still yield functional local planarization and passivation for devices in every region of the wafer in a single step.

#### IV. VARIATIONS ON OUR METHOD

Our method, as described in the previous section, mentions utilizing undercuts formed by etching while the hard mask is in place. It might be that some processes cannot accommodate undercuts easily, such as in the case of a particularly narrow waveguide. In this case, our method calls for retaining the hard mask once more, while the etch back now has to be stopped within the region between the top of the hard mask and the top of the critical epitaxial layer that requires passivation. For that, the hard mask thickness should be carefully chosen to be able to stop the etch back within the thickness of the hard mask.

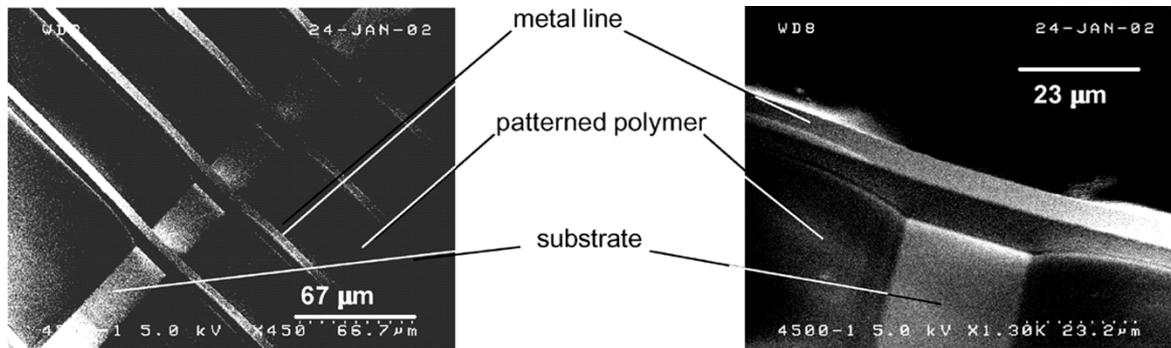


Fig. 8. SEM pictures of metal lines running continuously up and down the patterned BCB islands for device integration.

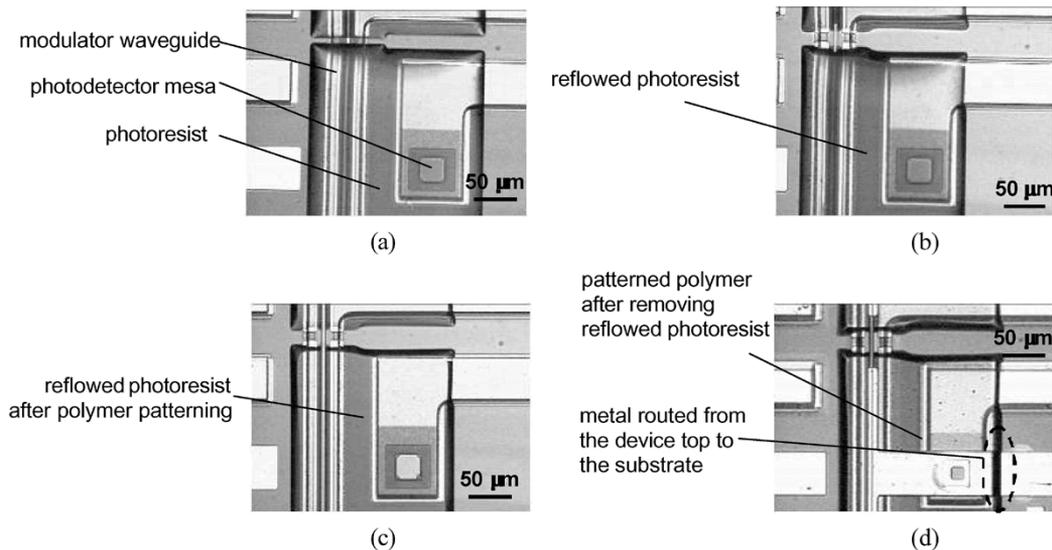


Fig. 9. Top-plan charge-coupled device pictures of on-chip integrated semiconductor devices with a reflowed photoresist mask over the passivation polymer (a) before and (b) after polymer etch, and with the resulting BCB pattern (c) after the photoresist mask is removed and (d) after the top metal is laid down.

The hard-mask-assisted planarization method is particularly suited to create locally perfectly leveled structures. In the case that planarization is not needed and the only purpose for the use of the polymer is sidewall passivation, another variation on this method can be adapted as follows. The polymer etch back is stopped when the substrate surface is reached. After the etch back, due to the roof protection, a thin layer of polymer on the sidewalls is obtained. This forms a thin wall of passivation layer, as sketched in Fig. 7. This is a convenient, fast method of passivation that has only spinning and curing steps and a time-insensitive etching step, as long as care is taken that the hard mask holds up to the spinning and curing steps.

Beyond passivation and planarization, for integration purposes, devices typically need to be connected to metal lines that then should be routed to the appropriate location, for example, to another device, on the wafer. In some cases, the designer might want to route a metal layer to a different horizontal level, for instance, from the top of the device down to the substrate level, with proper isolation. An additional step on the process described above can provide the required path for such multilevel metal routing. Once the polymer is etched down to the desired level for planarization and the hard mask is re-

moved, another polymer patterning step is performed, utilizing a reflowed photoresist mask. During this step, the unmasked polymer regions are removed completely. Due to the particular initial profile of the reflowed photoresist and the polymer being eaten away at etch edges, the resulting polymer profile is an extremely smooth, gentle angle sloping down to the substrate level from the top of the planarization. Thus, when subsequent metallization is carried out, a continuous, good quality metal line is laid out, as demonstrated in Fig. 8. For device-to-device interconnects, the metal line might also be allowed to lie on the polymer at the planarization level. Fig. 9 shows different stages of BCB patterning and metallization for on-chip device integration.

Our method is particularly powerful because it can utilize the same polymer for multiple purposes. In addition to passivation, planarization, and routing of metal lines as described above, we also note for the waveguide devices that the use of the passivation polymer surrounding the waveguide ridge allows for a waveguide design with a higher refractive index cladding. As a result, single-mode propagation can be achieved through the waveguide structures that are wider than those with air claddings. Furthermore, the use of polymer surrounding the

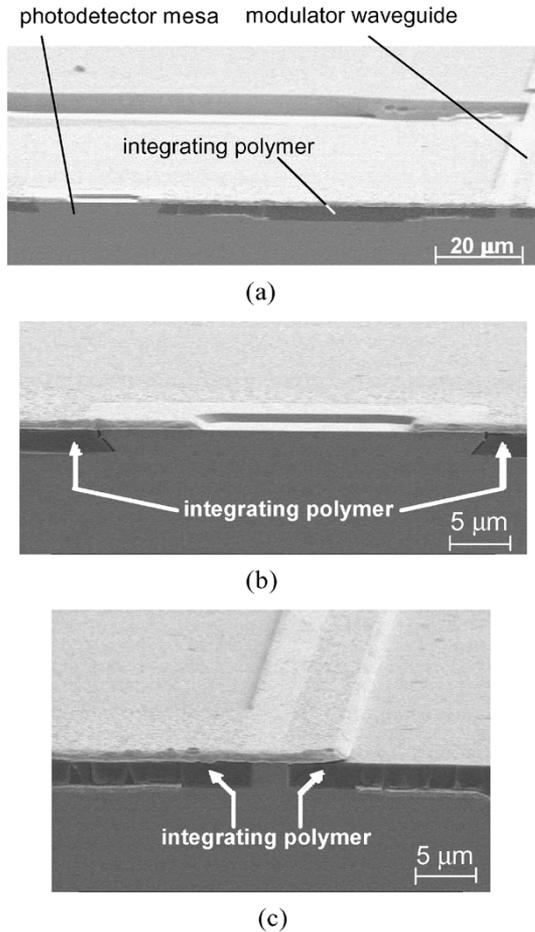


Fig. 10. Cross-sectional SEM picture of (a) on-chip integrated photodiode and modulator using BCB as the integrating polymer, (b) photodiode, and (c) modulator.

semiconductor ridge reduces the optical scattering from the roughness of the ridge sidewalls compared to the scattering from the semiconductor/air interface, yielding lower waveguide loss.

## V. APPLICATION OF OUR METHOD

We applied the method of self-aligning hard-mask-assisted passivation and planarization to the on-chip integration of a III–V photodiode/quantum well modulator system (PD/QWM). With such chip-scale PD/QWM integration, we fabricated an InP-based photonic switch and wavelength converter for telecommunication applications [3]–[5]. To the best of our knowledge, the integration of a surface-normal PD and a lumped QWM with the use of a passivation and planarization polymer (BCB in this case) had never been previously implemented on a single substrate.

The on-chip photodiode and modulator integration, shown in Fig. 10, introduced different requirements and functional uses of the chip passivation and planarization: 1) Both the photodiode mesa and the quantum-well modulator waveguide required sidewall passivation. The passivation was provided by the BCB coverage; 2) To achieve a single-mode waveguide for the modulator with a wider ridge structure, the waveguide was fabricated with the BCB-cladding for the horizontal direction,

TABLE I  
FAST AND SLOW ETCH RECIPES FOR THE ETCH BACK OF BCB

Parameter	Fast Etch	Slow Etch
	1.4–1.6 $\mu\text{m}/\text{min}$	0.4–0.6 $\mu\text{m}/\text{min}$
$\text{O}_2$	100 sscm	100 sscm
$\text{CHF}_3$	20 sscm	5 sscm
He	5 sscm	5 sscm
Pressure	30 mTorr	30 mTorr
Bias	50 V	50 V
UHF Power	1700 W	1700 W

Etching was done using the Nextral 8000 plasma etcher.

rather than the air-cladding (In the vertical direction, a specially included epitaxial layer provided the cladding.); 3) The QWM featured an electrical connection in the form of a metal line lying on top of the waveguide. Since the resultant waveguide was only  $2 \mu\text{m}$  wide, its metal line made use of the physical support from below, provided by the BCB surrounding the ridge; 4) The photodiode and modulator were electrically connected through a high-speed metal interconnect, which went through the shortest path possible between the tops of the two devices, supported by the BCB layer. Creating electrical connections to this metal line from the photodiode and the modulator was enabled with the planarization around both devices, as well as clean connection surfaces at their top surfaces; 5) Since the photodiode was formed by a second growth, it ended up being  $0.5 \mu\text{m}$  higher than the QWM due to regrowth enhancement. Our hard mask-assisted passivation and planarization technique, with BCB as the polymer, was used for simultaneous local planarization of both devices; 6) The circuit of the photonic switch incorporated another electrical component, which is connected to the devices through another interconnect. This interconnect was laid over a gently sloping BCB layer from the top of the required device, the slope being formed by the method described in the previous section; and 7) The layout also featured, at places, different metal lines biased at different dc levels tens of volts apart, running at different horizontal levels. Such large dc voltage application was possible because of the good on-chip electrical isolation achieved by BCB separating the two levels.

We used Cyclotene 3022-63, the most viscous type of BCB, and spun at 5000 r/m for 80 s on the wafer pieces following the guidelines in [6]. The wafer piece was then hard cured at  $250^\circ\text{C}$  under nitrogen purge using the temperature profile suggested by the manufacturer [6]. This rendered a  $9\text{--}10\text{-}\mu\text{m}$ -thick film of BCB with a thickness nonuniformity of  $\pm 0.1 \mu\text{m}$  for  $3\text{-}\mu\text{m}$  deep waveguide ridges ( $2 \mu\text{m}$  wide) and mesas ( $30 \times 30 \mu\text{m}$  in size). For the etch back, we applied a fast etch recipe with an etch rate of  $1.4\text{--}1.6 \mu\text{m}/\text{min}$  and a consecutive slow etch recipe with an etch rate of  $0.4\text{--}0.6 \mu\text{m}/\text{min}$ . Table I gives the details of these etch recipes. These recipes yielded anisotropic etches, as necessary to prevent the BCB surrounding the device structures from undercutting.

The fabricated switches exhibited good performance during our characterization and testing. The successful switch operation demonstrated the effectiveness of BCB and hard-mask-as-

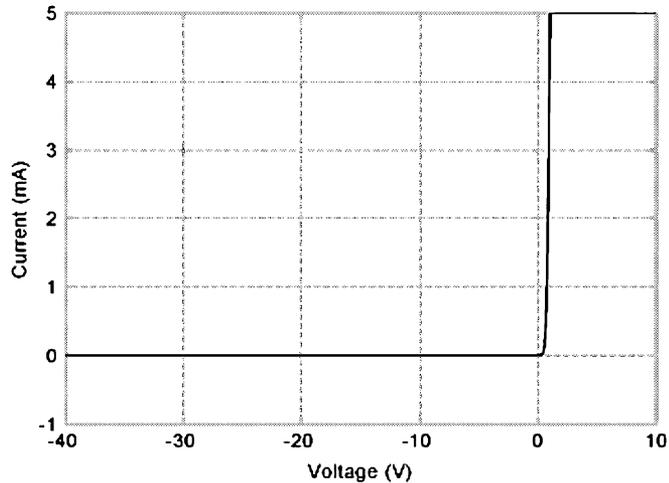


Fig. 11. IV curve of a passivated InP diode.

sisted passivation and planarization. The breakdown voltage, rated at  $1\ \mu\text{A}$  of dark current for the  $30\times 30\ \mu\text{m}$ ,  $3\text{-}\mu\text{m}$  high photodiode mesa with a  $1.5\text{-}\mu\text{m}$ -thick intrinsic region was  $\sim 30\ \text{V}$ . For the  $2\text{-}\mu\text{m}$ -wide  $300\text{-}\mu\text{m}$ -long  $3\text{-}\mu\text{m}$  deep-etched modulator waveguide with a  $0.5\text{-}\mu\text{m}$ -thick intrinsic region, it was  $\sim 20\ \text{V}$ . The avalanche breakdown typically occurred at  $>35$  and  $>25\ \text{V}$  for the photodiode and the modulator, respectively. Fig. 11 shows a current–voltage curve of such a BCB-passivated diode, with an avalanche breakdown of  $>40\ \text{V}$ . The high breakdown voltages and low leakage currents observed for the devices demonstrated successful passivation of the photodiode and modulator. It was possible to extract a maximum photocurrent of  $8\ \text{mA}$  from the photodiode, implying that there were no excessive leakage currents, unwanted breakdowns, imperfect isolation, and other undesirable electrical characteristics present in the structure. The ohmic contacts for the integrated diodes were measured to be  $\sim 10\ \Omega$ , indicating that the contact surfaces were smooth and free of contamination, as the hard mask guaranteed. In spite of device heights being different by  $0.5\ \mu\text{m}$ , which would ordinarily complicate the simultaneous planarization and result in low fabrication yield for such a structure, by using our self-aligning hard-mask-assisted planarization method, we achieved a yield of  $>90\%$ . Through postetch patterning of the BCB layer, we routed metal lines from the top of the modulator to the electrical component on the substrate  $3\ \mu\text{m}$  below. Such multifunctional use of the BCB passivation layer was the key to our efficient on-chip device integration.

This technique can also be utilized in other device architectures of different material systems where the planarization of vertical structures is necessary. For example, high electron mobility transistors (HEMT) typically require planarization of the gate electrodes with the drain and source electrodes such that the transistors can be interconnected properly to make an integrated circuit (IC). The variation in the height of the gates across the wafer, however, makes this task harder, reducing the yield. Because of its decreased sensitivity to the height variation, our technique could be useful also for HEMT-ICs to improve the yield.

## VI. CONCLUSION

By the development and utilization of a self-aligning hard-mask-assisted passivation and planarization method, we fabricated a functional photonic switch that showcases several beneficial features of our method. We achieved good quality passivation and metal-to-device connections, perfect local planarization in a single-etching step even with devices of different heights integrated on a single wafer, high process yield in spite of through-the-wafer process variations in polymer thickness and etch rate, and versatile interconnections with good isolation between metal lines at different bias levels. This method is convenient because: 1) it makes use of the hard mask layer already present to define the devices without requiring an extra mask step and 2) a single step achieves reliable, high-yield self-aligning planarization and passivation for devices in all regions of a wafer. The method is also versatile; it can be modified as was described to accommodate different design requirements and targets.

## ACKNOWLEDGMENT

The authors would like to thank Intel Corporation for allowing the use of Nextral 8000 and Melles Griot for providing a waveguide alignment setup.

## REFERENCES

- [1] Y.-H. So, P. Garrou, J.-H. Im, and D. M. Scheck, "Benzocyclobutene-based polymer for microelectronics," *Chemical Innovation*, vol. 31, no. 12, pp. 40–47, 2001.
- [2] J.-F. Zheng, J. P. Hanberg, H. V. Demir, V. A. Sabnis, O. Fidaner, J. S. Harris Jr., and D. A. B. Miller, "Novel passivation and planarization in the integration of III–V semiconductor devices," in *Proc. SPIE Photonics West Conf.*, San Jose, CA, Jan. 24–29, 2004.
- [3] H. V. Demir, V. A. Sabnis, O. Fidaner, J. S. Harris Jr., D. A. B. Miller, J.-F. Zheng, N. Li, T.-C. Wu, and Y.-M. Houg, "Novel scalable wavelength-converting crossbar," in *Proc. IEEE-OSA Optical Fiber Communications Conf. (OFC)*, Los Angeles, CA, Feb. 22–27, 2004.
- [4] H. V. Demir, V. A. Sabnis, O. Fidaner, S. Latif, J. S. Harris Jr., D. A. B. Miller, J.-F. Zheng, N. Li, T.-C. Wu, and Y.-M. Houg, "Novel optically-controlled optical switch based on intimate integration of surface-normal photodiode and waveguide electroabsorption modulator for wavelength conversion," in *Conf. Lasers and Electro-Optics (LEOS)*, Tucson, AZ, Oct. 26–30, 2003, pp. 644–645.
- [5] H. V. Demir, V. A. Sabnis, O. Fidaner, J. S. Harris Jr., D. A. B. Miller, and J.-F. Zheng, "Dual-diode quantum-well modulator for C-band wavelength conversion and broadcasting," *OSA Opt. Express*, vol. 12, no. 2, pp. 310–316, 2004.
- [6] "Processing Procedures for Dry-Etch Cyclotene Advanced Electronics Resins," Dow Chemicals, Tech. Rep.
- [7] M. A. Herman and S. Helmut, *Molecular Beam Epitaxy: Fundamentals and Current Status*, 2nd ed. New York: Springer, 1996.
- [8] G. B. Stringfellow, *Organometallic Vapor-Phase Epitaxy: Theory and Practice*. Boston, MA: Academic, 1989.
- [9] T. Van Caenegem, I. Moerman, and P. Demeester, "Selective area growth on planar masked InP substrates by metal organic vapor phase epitaxy (MOVPE)," *Prog. Crystal Growth Charact.*, vol. 35, no. 2–4, pp. 263–288, 1997.
- [10] R. E. Williams, *Gallium Arsenide Processing Techniques*. Dedham, MA: Artech, 1984.
- [11] S. Sloan, "Processing and passivation techniques for fabrication of high-speed InP/InGaAs mesa photodetectors," *Hewlett-Packard J.*, pp. 69–75, Oct. 1989.
- [12] J. D. Robinson and B. Humphreys, "Plasma etch optimization of a photo-sensitive benzocyclobutene (BCB) planarization layer for photonic integrated circuit manufacturing," MetroPhotonics, Inc., Tech. Rep., Apr. 2003.



**Hilmi Volkan Demir** (S'98) received the B.Sc. degree in electrical and electronics engineering from Bilkent University, Ankara, Turkey, in 1998, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 2000 and 2004, respectively.

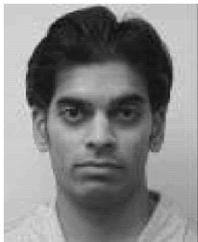
At Stanford University, his doctoral research under Professors D. A. B. Miller and J. S. Harris, Jr., focused on invention, design, fabrication, testing, and modeling of multifunctional integrated photonic switches; his Ph.D. thesis led to the world's first wavelength-converting crossbar switches. In September 2004, he joined Bilkent University, where he is currently an Assistant Professor of Physics. He is also an Associate Director of Bilkent Nanotechnology Research Center and a faculty member of the Bilkent Advanced Research Laboratory. He has published more than 20 journal and conference papers, and has presented more than ten invited talks, co-translated two books, and disclosed four U.S. patents (two filed, one allowed, one continuation).

Dr. Demir is a recipient of the Stanford Intel Research Assistantship (2000–2004), the Edward L. Ginzton Fellowship (1998–1999), and the Bilkent Board of Trustees Scholarship (1994–1998). He was one of the Stanford-Berkeley Innovator's Challenge Finalists, in 2003, and an invited participant of London International Youth Science Forum, U.K., in 1994.



**Jun-Fei Zheng** received the Ph.D. degree in materials science from University of California, Berkeley, in 1994.

Since then he has been with Intel Corporation, Santa Clara, CA, working on silicon process technology development, advanced MOS transistors, and photonic and optoelectronic devices. Currently, he is with the Strategic Technology Group and an Intel researcher-in-residence at Stanford University, Stanford, CA.



**Vijit A. Sabnis** received the B.Sc. degree (highest honors) in electrical engineering and computer sciences from the University of California, Berkeley, in 1995 and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1997 and 2003, respectively.

His doctoral research was conducted in the areas of epitaxial growth, fabrication, simulation, and characterization of optically controlled electroabsorption modulators. He is currently with Translucent, Inc.



**Onur Fidaner** (S'00) received the B.Sc. degree in electrical and electronics engineering from Middle East Technical University (METU), Ankara, Turkey, in 2001, and the M.S. degree in electrical engineering from Stanford University, Stanford, CA in 2003. He is currently working toward the Ph.D. degree at the same university.

He is a Lucent Technologies Stanford Graduate Fellowship Student at Stanford University. His research interests include development of novel ultrafast photonic devices incorporating quantum well structures for future optical networks.



**Jesper Hanberg** received the B.S. and Ph.D. degrees in physics from University of Copenhagen, Copenhagen, Denmark, in 1983 and 1987, respectively.

Presently he is with Giga ApS, Intel Corporation, Skovlunde, Denmark, working with design, fabrication, and integration of high-speed opto-electronic components.



**James S. Harris, Jr.** (F'88) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1964, 1965, and 1969, respectively.

He is the James and Ellenor Chesebrough Professor of Engineering at Stanford University. In 1969, he joined the Rockwell International Science Center, Thousand Oaks, CA, where he was one of the key contributors in developing their preeminent position in GaAs device technology. In 1982, he joined the Solid State Electronics Laboratory,

Stanford University, as a Professor of electrical engineering. He served as the Director of the Solid State Electronics Laboratory, Stanford University, from 1981 to 1988. His current research interests include the physics and application of ultra-small structures to new electronic and optoelectronic devices and high-speed integrated circuits and MBE growth coupled with a scanning-probed-induced oxidation for fabrication of nano three-dimensional structures. He has more than 500 publications in these areas.

Dr. Harris, Jr., is a Fellow of the American Physical Society and he received the Heinrich Walker medal, IEEE Third Millennium Medal, and the 2000 IEEE Morris N. Liebmann Memorial Award for his contributions to GaAs devices and technology.



**David A. B. Miller** (M'84–SM'89–F'95) received the B.Sc. degree from St. Andrews University, U.K., and the Ph.D. degree from Heriot-Watt University, in 1979.

He was with Bell Laboratories, from 1981 to 1996, as a Department Head from 1987 to 1996 in the Advanced Photonics Research Department. He is currently the W. M. Keck Professor of Electrical Engineering at Stanford University, Stanford, CA, and the Director of the Ginzton and Solid State and Photonics Laboratories, Stanford, CA. His research interests include quantum-well optoelectronic physics and devices and fundamental and applications of optics in information, sensing, switching, and processing. He has published more than 200 scientific papers and holds over 40 patents.

Dr. Miller has served as a Board member for both the Optical Society of America (OSA) and IEEE Lasers and Electro-Optics Society (LEOS) and in various other society and conference committees. He was President of the IEEE Lasers and Electro-Optics Society in 1995. He was awarded the Adolph Lomb Medal and the R. W. Wood Prize from the OSA, the International Prize in Optics from the International Commission for Optics, and the IEEE Third Millennium Medal. He is a Fellow of the Royal Societies of London and Edinburgh, OSA, and APS and holds honorary degrees from the Vrije Universiteit Brussel and Heriot-Watt University.